DERWENT-ACC-NO: **2002-250428**

DERWENT-WEEK: 200230

TITLE: Trench isolation method using sige epitaxial layer

INVENTOR: CHOI, C J; KIM, C S ; KIM, H S ; KOO, J H

PATENT-ASSIGNEE: SAMSUNG ELECTRONICS CO LTD[SMSU]

PRIORITY-DATA: 1999KR-0028402 (July 14, 1999)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
KR 2001009810 A	February 5, 2001	N/A	001	H01L 021/76

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
KR2001009810A	N/A	1999KR-0028402	July 14, 1999

INT-CL (IPC): H01L021/76

ABSTRACTED-PUB-NO: KR2001009810A

BASIC-ABSTRACT:

NOVELTY - A **trench isolation** method using a **silicon**-germanium **epitaxial** layer
is provided to prevent the creation of interstitial **silicon** atoms in a **silicon**
substrate around the trench.

DETAILED DESCRIPTION - After a pad oxide layer(12) is formed on a silicon

substrate(10), a mask pattern(14) is formed thereon to define a trench region.
The substrate(10) is then etched to some depth through the mask pattern(14) to
form a trench. Thereafter, a silicon-germanium layer(30') is formed in the
trench and on the mask pattern(14) by epitaxial growth. In addition, a
sidewall oxide layer(34) of silicon oxide is formed on the silicon-germanium
layer(30') by thermal oxidation. Here, while the original silicon-germanium
layer(31) is thinner, another silicon-germanium layer(32) having a low silicon
content is formed between the original silicon-germanium layer(31) and the
silicon oxide layer(34). Therefore, interstitial silicon atoms can be hardly
created in the substrate(10) around the trench.

CHOSEN-DRAWING: Dwg.1/10

DERWENT-CLASS: L03 U11

CPI-CODES: L04-C12C;

EPI-CODES: U11-C08A3;

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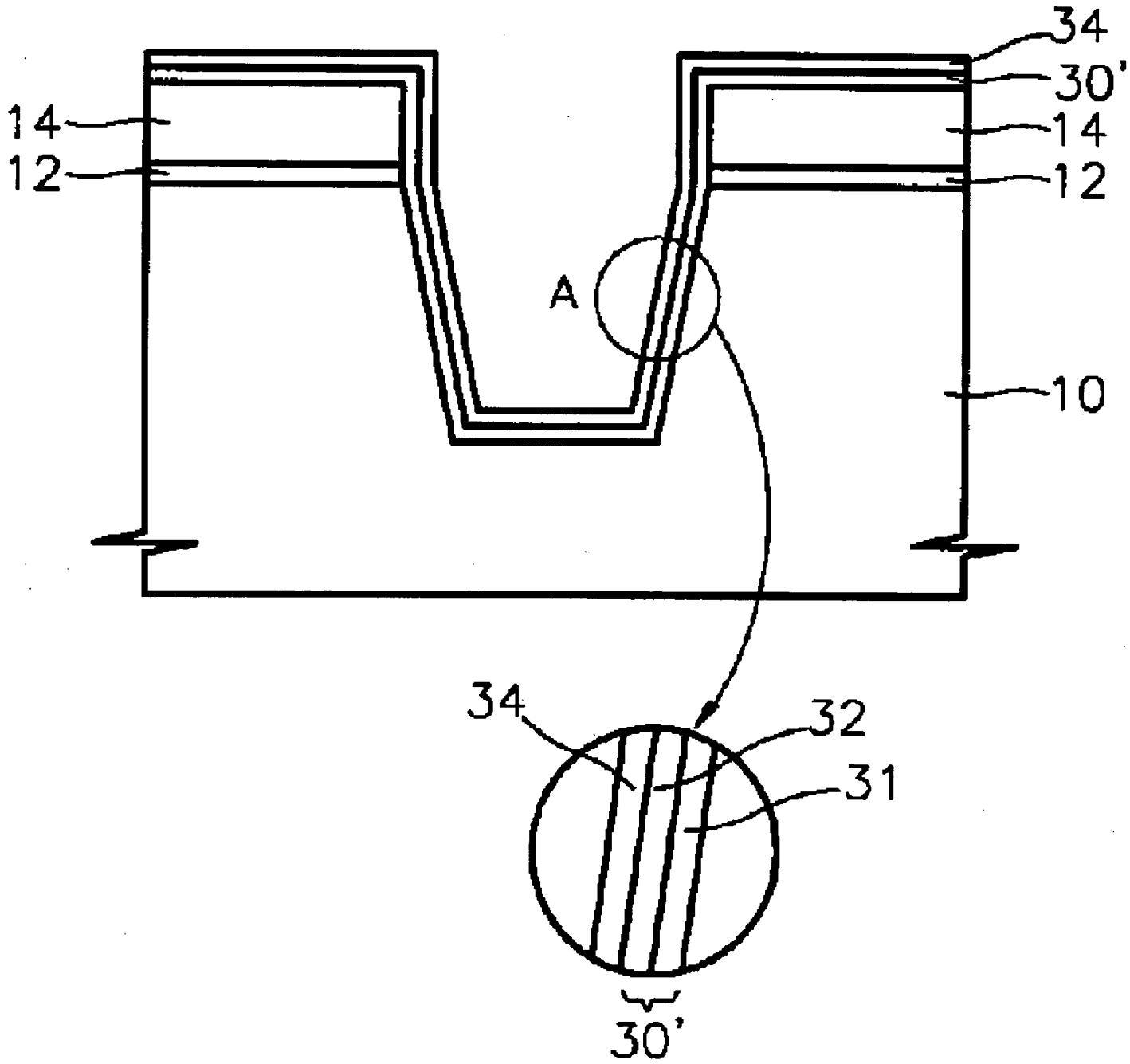
Basic Abstract Text - ABTX (1):
NOVELTY - A **trench isolation** method using a **silicon**-germanium **epitaxial**
layer is provided to prevent the creation of interstitial **silicon** atoms in a
silicon substrate around the trench.

Derwent Accession Number - NRAN (1):
2002-250428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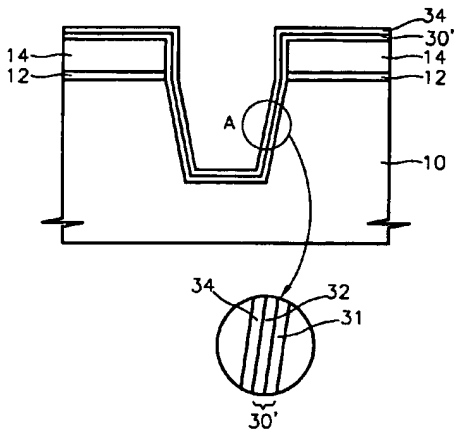
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